

## SYSTEMATIC DESIGN OF HIGH-SPEED AND LOW-POWER DIGIT-SERIAL MULTIPLIERS VLSI BASED

**Ms.P.J.Tayade\***

**Dr. Prof. A.A.Gurjar\*\***

### **Abstract:**

Terms of both latency and power Digit-serial implementation styles are best suited for implementation of digital signal processing systems which require moderate sampling rates. Digit-serial architectures obtain using traditional unfolding techniques cannot be pipelined beyond a certain level because of the presence of feedback loops. In this paper, an alternative approach for the design of digit-serial architectures is presented based on a novel design methodology. This methodology permits bit-level pipelining of the digit-serial architectures by moving all feedback loops to the last stage of the design. This enables bit-level pipelining of digit-serial architectures, thereby achieving sample speeds close to corresponding bit-parallel multipliers with lower area. This increased sample speed can be traded with reduction in power supply voltage resulting in significant reduction in power consumption. The proposed approach is applied to the design of various multipliers which form the backbone of digital signal processing computations. The results show that for transformed multipliers with smaller digit sizes ( $\leq 4$ ), the singly-redundant multiplier consumes the least power, and for larger digit sizes, the type-I multiplier consumes the least power. It is also found that the optimum digit size for least power consumption in type-I and type-III multipliers is  $\lfloor \frac{W}{2} \rfloor$ , where  $W$  represents the word length. Among the bit-level pipelined digit-serial multipliers, it is found that the redundant multiplier offers the best choice in consumption. The proposed digit-serial multipliers consume on average 20% lower power than the traditional digit-serial architectures for the non pipelined case and about 5–15 times lower power for the bit-level pipelined case.

**Keywords:** Bit-level pipelining, Booth recoding, carry-save arithmetic, digit-serial multiplier, low power, redundant arithmetic.

\* Electronics & telecommunication, Sipna's C.O.E.T., Amravati, India.

\*\* Electronics & telecommunication, Sipna's C.O.E.T., Amravati, India

## **INTRODUCTION:**

DIGITAL signal processing (DSP) is used in a wide range of applications such as telephone, radio, video, sonar, etc. The sample rate requirements vary from application to application and can range anywhere from 10 kHz to 100 MHz. Most of the DSP computations involve the use of multiply accumulate operations, and therefore the design of fast and efficient multipliers is imperative. Moreover, the demand for portable applications of DSP architectures has dictated the need for low-power designs. This is because the power consumption has a direct bearing on the lifetime of the batteries. For example, if the lifetime of the batteries can be reduced by a factor of half, the same number of batteries can now be used for twice the number of hours. Digit-serial multipliers are ideal for moderate-speed DSP computations and find many applications in heterogeneous high-level synthesis environments. Recently, it was found that digit-serial multipliers could be pipelined at the bit level thereby resulting in high processing speeds.

However, here the designs were obtained in an *ad hoc* manner. In this paper, based on and a systematic design methodology for low power digit-serial multipliers is presented. Traditionally, digit-serial multipliers were obtained by either folding the corresponding bit-parallel architectures or unfolding the bit-serial architectures. The architectures obtained in this manner cannot be pipelined at the bit-level. The approach presented in this paper enables the direct design of digit-serial architectures which can be pipelined at the bit-level. The advantage is two-fold. First, processing speeds comparable to a bit-parallel system can be obtained with less area. Second, since the critical path is reduced, the power supply voltage can be reduced for a fixed sampling frequency. This causes the proposed bit-level pipelined digit-serial architectures to consume lower power than the traditional digit-serial architectures.

## **Review of work:**

Yun-Nan Chang has presented a design methodology for a new class of digit-serial multiplier architectures. These architectures can be pipelined at the bit-level, and as a result power can be reduced. For a specified wsf, the clock speed required with a bit serial design is much higher than digit-serial with digit size 4 or 8. As a result, the power consumed by a bit-

serial design due to high-speed clock is much higher and this favors digit serial architectures with respect to low power consumption. It should also be noted that for large digit sizes.

**Digit-Serial Architectures using Unfolding Transformation** In this section, we motivate the need for digit-serial architectures, and present systematic design of digit-serial architectures using the unfolding Transformation. Consider the (word-serial) bit-serial implementation of the simple add operation. There are two approaches we can think of. First, we can process two input samples simultaneously, and process each input in a bit-serial manner; this corresponds to a word parallel bit-serial system with block size of two. Alternatively, we can process the inputs in a word serial manner, but process two bits of a word in parallel; this corresponds to a word-serial digit-serial implementation with digit-size.

### **Motivation:**

In parallel system speed, power is high and in addition area constraint is also high .To reduce the power and area we prefer bit serial architecture but it may be slow in speed, While we gain the power and area constraint but it loses the speed . So there is need of such a architecture which balance the both things from designer side, that is speed , power and area constraints .This is motivation to design a digit serial architecture.

### **Proposed work:**

Digit-Serial Architectures using the proposed design methodology is applied to various existing bit-serial multipliers including the type-I, type-II, type-III, and the singly-redundant multiplier.

#### **A.Type-I Multiplier:**

Consider the bit-serial type-I multiplier shown in Fig. 1 where the coefficient word length is four bits. This architecture contains four full adders, four multipliers, and some delay elements. In this multiplier, the carry-out signal of every adder is fed back after a delay to the carry-in signal of the same adder. The critical path of this architecture is full-adder delays. The traditional approach for designing the digit-serial architecture involves unfolding this structure by a factor

equal to the digit size . However, the resulting critical path would be full-adder delays; which can be further reduced to full-adder delays after pipelining. Reduction in the critical path below full-adder delays is *not possible* because of the presence of feedback loops. Therefore, in the final stage, a digit-serial adder is required to sum all these outputs. A simple digit-serial 3 : 2 compressor adder can be first used to reduce these three output digits to two digits. A digit-serial carry look-ahead adder or any other fast carry propagate adder is then used to add these two digits to generate the final result.

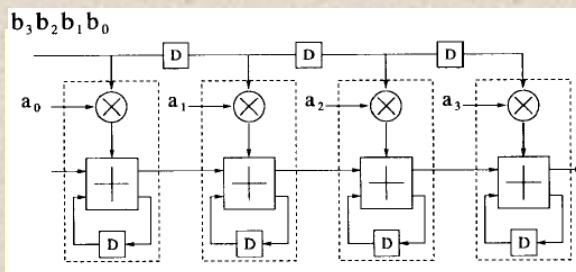


Fig.1-Type-I bit-serial multiplier with word length of 4 bits.

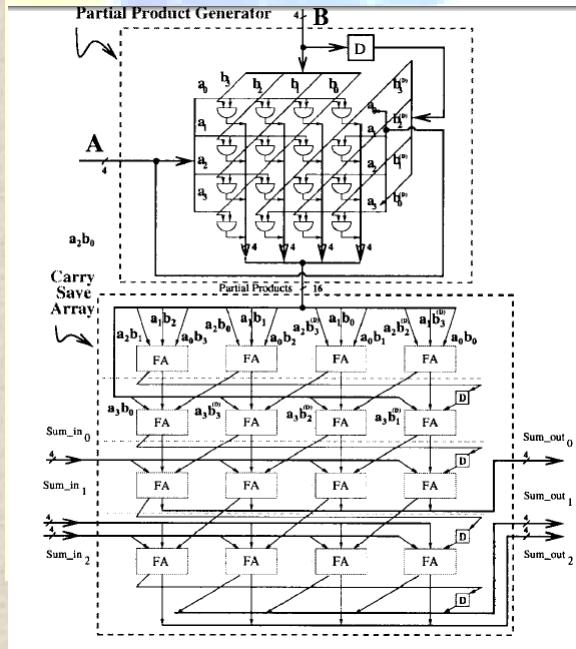


Fig. 2. Digit-cell for type-I multiplier.

**Type-II Multiplier:**

Consider the bit-serial type-II multiplier shown in Fig.3. The main difference between this multiplier and the type-I multiplier is that the critical path in this architecture is just two full-adder delays. Moreover, this architecture can be pipelined at the bit-level with an additional latency of only one clock-cycle unlike the type-I multiplier where the increase in latency would depend on the word length. If this architecture is unfolded using the traditional technique, the critical path would be full-adder delays. However, as in the case of the type-I multiplier, reduction in the critical path below is not possible due to the presence of feedback loops.

Fig. 5 is replaced with the digit-cell shown in Fig. 6. Here, represents the digit version of . For example, represents the four bits represents and so on. The partial product generator is identical to the one shown in Fig. 3. The entire digit-serial multiplier is designed by cascading these digit-cells similar to the type-I multiplier. A digit-serial 3 : 2 compressor and a carry look-ahead adder are required at the output of the last digit-cell to convert the three digit outputs to a single digit output.

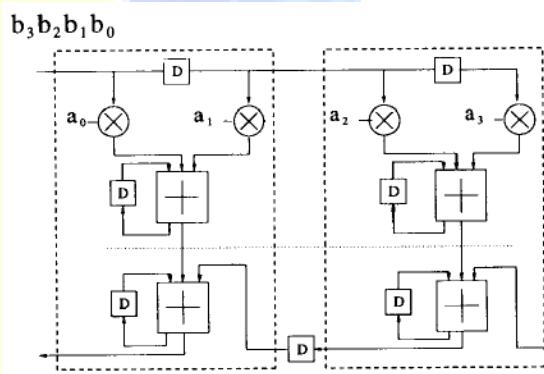


Fig. 3. Bit-serial type-II multiplier with word-length of 4 bits

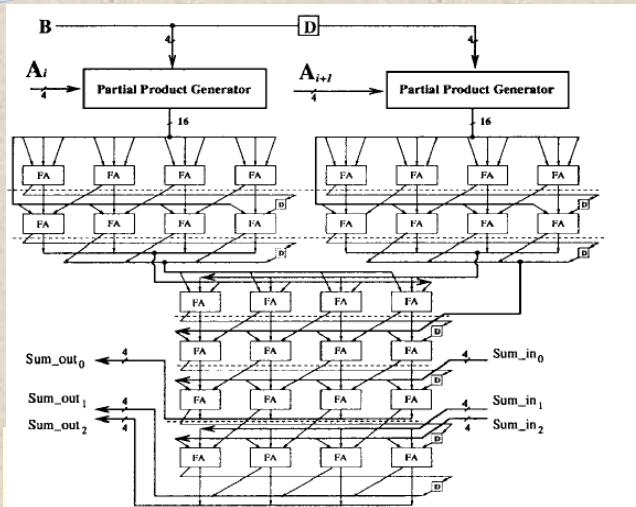


Fig. 4. Digit-cell for the type-II multiplier

### C. Type-III Multiplier

Consider the bit-serial type-III multiplier shown in Fig. 5. The salient feature of this architecture is that the carry-out signal is not fed back as in the type-I multiplier. If this architecture is unfolded using the traditional technique, the critical path would be full-adder delays. However in this case since there is no carry feedback, the unfolded architecture can also be pipelined at the bit-level. It should be noted that the partial product generator uses two coefficient digits and unlike the previous architectures where only one digit was used. It should also be noted that the carry-save portion generates four outputs at each stage. Therefore, at the output of the final digit-cell, a digit-serial 4 : 2 compressor and a fast carry look-ahead adder are required to convert the four digits to one digit. The resulting architecture can be pipelined at the bit-level.

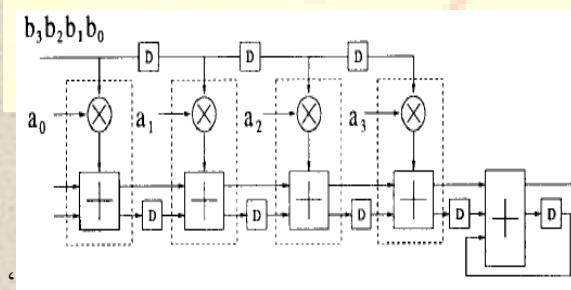


Fig.5 Bit-serial type-III multiplier with word-length of 4 bits.

## Conclusion:

This paper has presented a design methodology for a new class of digit-serial multiplier architectures. These architectures can be pipelined at the bit-level, and as a result power can be reduced. It should also be noted that for large digit sizes, the CSA module can be implemented using the Wallace tree algorithm. Experiments using HEAT tool showed that about 35% lower power is obtained for the non pipelined architecture using the Wallace tree approach when compared to the CSA-based architecture for a digit size of 8 and a word-length of 16 bits. For a specified wsf, the clock speed required with a bit serial design is much higher than digit-serial with digit size 4 or 8. As a result, the power consumed by a bit-serial design due to high-speed clock is much higher and this favors digit-serial architectures with respect to low power consumption. Note that the power consumed by the clock is not accounted for by the HEAT tool.

In this paper, comparison of critical path and power consumption of different digit-serial multipliers and their variation with respect to digit sizes have been explored. However, the comparison between the digit-serial and bit-parallel multipliers has not been addressed.

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